



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,374	12/16/2003	Roger Hansen	200312027-1	5369
22879 7590 09/20/2010 HEWLETT-PACKARD COMPANY Intellectual Property Administration 3404 E. Harmony Road Mail Stop 35 FORT COLLINS, CO 80528				
EXAMINER TRUONG, LOAN				
ART UNIT 2114		PAPER NUMBER		
NOTIFICATION DATE 09/20/2010		DELIVERY MODE ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

JERRY.SHORMA@HP.COM

ipa.mail@hp.com

laura.m.clark@hp.com

Office Action Summary

Application No.

10/737,374

Applicant(s)

HANSEN ET AL.

Examiner

LOAN TRUONG

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 38-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9, 38-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/22)
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date: _____

DETAILED ACTION

1. This office action is in response applicant's appeal brief filed June 30, 2010 in application 10/737,374.
2. Claims 1-9 and 38-41 are presented for examination. Claims 10-37 are previously cancelled.

Response to Arguments

3. Applicant's arguments with respect to claims 1-9 and 38-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-8 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanatham et al. (US 7,165,186) in further view of Traversat et al. (6,941,410) in further view of Kano et al. (US 7,222,194).

In regard to claim 1, Viswanatham et al. teaches a system for storing checkpoint data comprising:

a persistent memory unit (*backup store may be located on a separate computer from nodes 120A-B, fig. 1, col. 3 lines 53-56*) coupled to the network interface (*network may be a LAN, WAN, the internet or other types, col. 2 lines 63-67*), wherein:

the persistent memory unit (*backup store, fig. 1, 150*) is configured to receive the checkpoint data into a region of the persistent memory (*persistent store maybe able to store the current state of various active components, col. 3 lines 38-42*) via a remote memory write command (*execution of active component operate checkpoint mechanism to take checkpoint and store to persistent store, col. 4 lines 5-10*) from a primary process (*active application, col. 3 lines 20-28*) through the network interface unit (*network may be a LAN, WAN, the internet or other types, col. 2 lines 63-67*) and provide access to the checkpoint data in the region via a remote read command (*if server 130C fails sever 130B may be able to retrieved the saved state of component 144B, col. 4 lines 10-16*) from a backup process (*backup application, col. 3 lines 20-28*) through the network interface (*network may be a LAN, WAN, the internet or other types, col. 2 lines 63-67*); and

backup process provides recovery capability in the event of a failure of the primary process (*in the event of a server failure, the data objects may be retrieved by fail-over components on another server, col. 1 lines 35-41*).

Viswanatham et al. does not explicitly teach a persistent memory unit configured to receive or access data via a remote direct memory write/read.

Traversat et al. teach of a virtual heap for a virtual machine by implementing a virtual heap maintained on non-volatile memory storage external to the device running the virtual machine (*abstract*) and the virtual persistent heap enable the migration of the virtual machine computation states and thus the migration of executing processes from one machine to another (*abstract, fig. 5a*) implementing a paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

It would have been obvious to modify the system of Viswanatham et al. by adding Traversat et al. virtual heap. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would further teach the uses of the data in the persistent memory enable the check-pointing of the state of the computation of a virtual machine including processes executing within the virtual machine to a persistent storage (*abstract*).

Viswanatham et al. and Traversat et al. does not explicitly teach a network interface to an external network; and a persistent memory unit wherein the memory write command is preceded by a create request for the region and the read command is preceded by an open request for the region.

Kano et al. teach of a backup system constituted of a network attached storage (NAS) (*col. 3 lines 7-15*) wherein the NAS constituted of a network interface for connection to LAN (*fig. 1, 110*) wherein when a file access is for data write the NAS assigns a new data block for storing data (*col. 10 lines 7-26*) and when reception of an open command the backup server issues a file open request to the NAS (*col. 9 lines 63-67*).

It would have been obvious to modify the system of Viswanatham et al. and Traversat et al. by adding Kano et al. backup system. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would clearly show a connection of network such as a LAN through a network interface (*fig. 1, 110*) and further clearly describes method of file accesses (*col. 9 lines 43-67 and col. 10 lines 1-34*).

In regard to claim 2, Viswanatham et al. does not explicitly teach the system of Claim 1, further comprising: a persistent memory manager configured to program the network interface with information used by the network interface to perform virtual-to-physical address translation.

Traversat et al. teach the virtual heap with a page table and offset based address translation may be used to convert virtual heap references into in-memory heap references (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 3, Viswanatham et al. teach the system of Claim 1, wherein the persistent memory unit is configured to provide remote memory read to the checkpoint data to another processor, and the backup process is executed by the other processor (*if server 130C fails sever 130B may be able to retrieved the saved state of component 144B, col. 4 lines 10-16*).

Viswanatham et al. does not explicitly teach the system wherein the persistent memory unit provides data through a remote direct memory read.

Traversat et al. also provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 4, Viswanatham et al. teach the system of Claim 1, wherein the persistent memory unit provides the checkpoint data through remote memory reads by the backup process after the primary process fails (*in the event of a server failure, the data objects may be retrieved by fail-over components on another server, col. 1 lines 35-41*).

Viswanatham et al. does not explicitly teach the system wherein the persistent memory unit provides data through a remote direct memory read.

Traversat et al. also provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 5, Viswanatham et al. does not explicitly teach the system of Claim 1, wherein the persistent memory unit is configured to store multiple sets of checkpoint data through remote direct memory writes sent from the processor at successive time intervals.

Traversat et al. teach of a checkpoint be induced after a maximum elapsed time (*col. 24 lines 42-47*). Also, Traversat et al. provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 6, Viswanatham et al. does not explicitly teach the system of Claim 5, wherein the persistent memory unit provides the multiple sets of checkpoint data through remote direct memory reads upon request by the backup process at one time.

Traversat et al. teach of migrating a virtual persistent heap from one machine to another (*abstract*). Also, Traversat et al. provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 7, Viswanatham et al. teach the system of Claim 1, wherein the primary process provides the checkpoint data to the persistent memory unit independently from the backup process (*persistent store maybe able to store the current state of various active components, col. 3 lines 38-42*).

In regard to claim 8, Viswanatham et al. teach the system of Claim 1, wherein the persistent memory unit is configured as part of a memory access-enabled system area network (*network may be a LAN, WAN, the internet or other types, col. 2 lines 63-67*).

Viswanatham et al. does not explicitly a remote direct memory access.

Traversat et al. also provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

In regard to claim 39, Viswanatham et al. does not explicitly teach the system of Claim 1, the persistent memory unit configured to provide access to the checkpoint data in another region via a remote memory read command from the backup process (*sever 130B may be able to retrieved the saved state of component 144B, col. 4 lines 10-16*) through the network interface (*network may be a LAN, WAN, the internet or other types, col. 2 lines 63-67*).

Viswanatham et al. does not explicitly a remote direct memory access.

Traversat et al. also provide paging-based approach which may enable page protection mechanisms and support for DMA and block I/O devices (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

Viswanatham et al. and Traversat et al. does not explicitly teach the persistent memory unit wherein the read command is preceded by an open request for the another region.

Kano et al. teach of a file access is for data write the NAS assigns a new data block for storing data (*col. 10 lines 7-26*) and when reception of an open command the backup server issues a file open request to the NAS (*col. 9 lines 63-67*).

Refer to claim 1 for motivational statement.

In regard to claim 40, Viswanatham et al. does not explicitly teach the method of Claim 1, wherein the checkpoint data received by the persistent memory unit overwrites a current set of the checkpoint data.

Traversat et al. teach of persistent store space may include an entire copy of the virtual heap for one or more other applications (*col. 10 lines 23-34*).

Refer to claim 1 for motivational statement.

In regard to claim 41, Viswanatham et al. does not explicitly teach the method of Claim 1, wherein the checkpoint data received by the persistent memory unit is appended to a previous set of the checkpoint data.

Traversat et al. teach of persistent store space may include one or more versions of copies of virtual heap or checkpointed states (*col. 10 lines 23-34*).

Refer to claim 1 for motivational statement.

5. Claims 9 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanatham et al. (US 7,165,186) in further view of Traversat et al. (6,941,410) in further view of Kano et al. (US 7,222,194) in further view of DeKoning (US 6,691,245).

In regard to claim 9, Viswanatham et al does not explicitly teach the system of Claim 1, wherein the persistent memory unit is configured with translation tables.

Traversat et al. teach the virtual heap with a page table and offset based address translation may be used to convert virtual heap references into in-memory heap references (*col. 19 lines 23-31*).

Refer to claim 1 for motivational statement.

Viswanatham et al., Traversat et al., and Kano et al. does not explicitly teach the system of Claim 1, wherein the persistent memory unit is configured with address protection to authenticate requests from remote processors, and to provide access information to authenticated remote processors.

DeKoning teach of a remote storage device which is initially fully mirrored from the local storage device before operations can start using the local host device (*col. 7 lines 58-65*).

It would have been obvious to modify the system of Viswanatham et al. and Traversat et al. and Kano et al. by adding DeKoning host-initiated and fail-over. A person of ordinary skill in the art at the time of applicant's invention would have been motivated to make the modification because it would provide the second host device upon failure of the first host device to initiate a switch or fail-over and server as the

primary on behalf of the client devices (*abstract*).

In regard to claim 38, Viswanatham et al., Traversat et al., and Kano et al. does not explicitly teach the system of Claim 1, wherein the persistent memory unit is further configured to store meta-data regarding the contents and layout of memory regions within the persistent memory unit and to keep the meta-data consistent with the checkpoint data stored on the persistent memory unit.

DeKoning teach of a primary storage device stores data received from the host device responds to the storage access request and at a synchronize checkpoints forward the data and the synchronization checkpoint to the secondary storage (*col. 4 lines 1-8*).

Refer to claim 9 for motivational statement.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 10am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
AU 2114

/Scott T Baderman/
Supervisory Patent Examiner, Art Unit
2114